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10EC63

Sixth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting at least TWO questions from each part.*
2. State all assumptions, including missing data.

PART – A

1 a. Derive an expression for drain-to-source current i_{DS} from i_D v/s V_{DS} relationship for triode and saturation regions of n-MOSFET. **(10 Marks)**

b. For an 0.8μm technology for which t_{OX} = 15nm, μ_n = 550 cm^2/V. Find k'_n and c_{OX} and the overdrive voltage $V_{ov} = V_{as} - V_t$ required to operate a transistor having W/L = 20 in saturation with I_D = 0.2 mA. What is the minimum V_{DS} needed? **(06 Marks)**

c. Design the circuit shown in Fig.Q.1(c) to obtain a drain voltage of 0.1V. What is the effective resistance between drain and source? At this operating point, let V_t = 0.8V and $K_n^1\left(\frac{W}{L}\right) = 1mA/V^2$. **(04 Marks)**

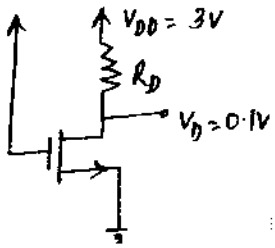

Fig.Q.1(c)

2 a. Briefly explain any two types of biasing methods in MOS amplifier circuits. **(06 Marks)**

b. For a common source amplifier with g_m = 2 mA/V, r_0 = 50KΩ and R_D = 10KΩ, R_G = 10MΩ, R_L = 20KΩ and R_{sig} = 0.5MΩ. Calculate R_{in}, G_v, A_v, A_{vo}, R_{out}. **(10 Marks)**

c. Mention any 4 comparison of important characteristics of MOSFET and the BJT. **(04 Marks)**

3 a. Explain the CMOS implementation of IC common source amplifier and hence explain how to determine its small signal voltage gain. **(10 Marks)**

b. For the common gate amplifier with W/L = 4μm/0.2μm, $\mu_n C_{OX}$ = 350 $\mu A/V^2$, r_0 = 18 KΩ, I_D = 100μA, g_m = 1.2 mA/V, χ = 0.2, R_s = 10KΩ, R_L = 100 KΩ, C_{gs} = 20fF, C_{gd} = 5fF, C_L = 5fF. Find A_{vo}, R_{in}, R_{out}, G_v, G_{is}, G_i and f_H. **(10 Marks)**

4 a. Explain the circuit of MOS cascade amplifier and hence obtain an expression for short circuit transconductance G_M. **(10 Marks)**

b. Explain briefly with neat circuit diagrams:
i) Wilson MOS mirror
ii) Widlar current source. **(10 Marks)**

PART – B

5 a. Explain the basic operation of BJT differential pair. **(08 Marks)**

b. For the nMOS differential pair with a common-mode voltage V_{cm} applied as shown in Fig.Q.5(b). let $V_{DD} = V_{SS} = 2.5V$, $K_n' W/L = 3mA/V^2$, $V_{tn} = 0.7V$, $I = 0.2mA$, $R_D = 5K\Omega$. Neglect channel length modulation.

i) Find V_{OV} and V_{GS} for each transistor.

ii) For $V_{CM} = 0$ find V_s, i_{D1}, i_{D2}, V_{D1} and V_{D2}.

iii) Repeat (ii) for $V_{cm} = 1V$.

iv) What is the highest value of V_{cm} for which Q_1 and Q_2 remain in saturation, if current source I requires a minimum voltage of 0.3V to operate properly. What is the lowest value for V_s and hence for V_{cm}. **(12 Marks)**

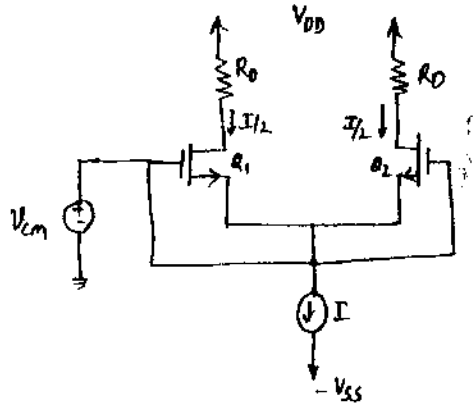

Fig.Q.5(b).

6 a. Explain briefly with expressions the properties of negative feedback. **(08 Marks)**

b. A series-shunt feedback amplifier employs a basic amplifier with input and output resistances each of 1KΩ and gain A = 2000 V/V. The feedback factor β = 0.1 V/V. Find the gain A_f the input resistance R_{i_f} and output resistance R_{o_f} of the closed loop amplifier. **(06 Marks)**

c. Explain briefly an alternative approach for finding loop gain Aβ. **(06 Marks)**

7 a. Explain instrumentation amplifier with neat circuit diagrams. **(08 Marks)**

b. With neat diagram, explain the sample and hold circuit using opamp. **(07 Marks)**

c. Derive an expression for an input resistance of the inverting amplifier taking into account the finite open loop gain A of the opamp shown in Fig.Q.7(c). **(05 Marks)**

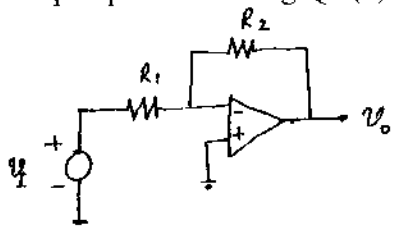

Fig.Q.7(c)

8 a. Briefly discuss the parameters used to characterize the operation and performance of logic circuit families. **(08 Marks)**

b. Write the expressions for propagation delay of an inverter. **(05 Marks)**

c. Sketch a CMOS logic circuit that realizes the function $Y = AB + \overline{AB}$ using equivalence or co-incidence function. **(07 Marks)**

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